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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
ROMAN, ANGEL

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 06/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/816,962	PING ET AL.	
	Examiner	Art Unit	
	Angel Roman	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-100* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *72-78* is/are allowed.

6)☒ Claim(s) *1-71 and 79-100* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Objections

1. Claim 92 is objected to because of the following informalities: "an-type" should be replaced with --an n-type--. Appropriate correction is required.

2. Claim 41 objected to because of the following informalities: In line 1, "of" should be deleted. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 3, 4 and 79 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claims 3 and 4 recite the limitation "the silicon substrate" in the first line of the claims. There is insufficient antecedent basis for this limitation in the claim.

6. Claim 79 recites the limitation "the horizontal surface" in line 6. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

8. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

9. Claim 47 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Withek et al. U.S. Patent 5,393,681.

Withek et al. discloses a method of forming a vertical structure on a substrate, comprising; forming multiple overlying epitaxial layers having insulated sidewalls and a top surface (see figure 32).

10. Claims 1, 8, 32, 33, 35, 44 and 45 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakamura U.S. Patent 6,391,692.

Nakamura discloses a method of forming a vertical structure on a substrate 12, comprising the steps of; selectively growing a first epitaxial layer 13 of monocrystalline silicon on the substrate 12; forming a layer 48 of an insulative material over the first epitaxial layer 13; removing a portion of the insulative layer to expose only a top surface of the first epitaxial layer (see figure 4); selectively growing a second epitaxial layer 51 of monocrystalline silicon on the exposed surface of the first epitaxial layer 13; and forming a layer 52 of an insulative material over the second epitaxial layer (see figure 5e).

One or more of the epitaxial layers having a thickness of about 70 to about 100 nm (see column 5, lines 11-13).

The insulative layer comprises oxide, nitride, oxidized nitride, or a composite oxide/nitride (see column 5, lines 3-10).

The insulative layer comprises silicon nitride or silicon oxide (see column 4, lines 44-46).

The vertical structure is formed adjacent to an existing gate 46 or word line on the substrate (see figure 4).

The existing gate or word line is electrically isolated by region 44 (see figure 4).

11. Claims 83-85, 88-91, 93, 95, 97 and 99 are rejected under 35 U.S.C. 102(b) as being anticipated by Mazuré et al. U.S. Patent 5,308,782.

Mazuré et al. discloses a method of forming an elevated transistor in a semiconductive wafer processing comprising the steps of providing a semiconductor substrate; forming a buried drain in the substrate; forming an elevated gate over the buried drain by the steps of forming a first epitaxial layer over the buried drain; forming an insulative layer over the first epitaxial layer; removing a portion of the insulative layer to expose only a horizontal surface of the first epitaxial layer; forming a second epitaxial layer over the first epitaxial layer; forming an insulative layer over the second epitaxial layer; and repeating the foregoing steps to form additional overlying epitaxial layers to form a pillar-like structure having a desired height; each epitaxial layer having insulated sidewalls, and the uppermost epitaxial layer having an exposed horizontal surface; and forming a source region onto the gate by forming at least one epitaxial layer over the uppermost epitaxial layer, while doping (see figures 15-20).

The step of forming the buried drain comprises doping an area of the substrate with an n-type dopant by ion implantation.

The step of forming the source region comprises doping the at least one epitaxial layer with an n-type dopant

Mazuré et al. also discloses a method of processing a semiconductor wafer, comprising forming an elevated transistor by the steps of; providing a semiconductor substrate 12; forming a buried drain 14 in the substrate forming an elevated gate 34

over the buried drain 14, the gate comprising multiple overlying epitaxial layers in a vertical orientation with each epitaxial layer having insulative sidewalls (see figure 12); and forming a source region (54, 56) over the uppermost epitaxial layer of the gate, the source region comprising one or more epitaxial layers, each layer having insulative sidewalls (see figure 14) and the uppermost layer having an insulated top surface (see figure 19).

The step of forming the elevated gate comprises; depositing an epitaxial layer above the buried drain; depositing a layer of insulative material over the epitaxial layer; removing a horizontal surface of the insulative layer to expose the epitaxial layer; and repeating the foregoing steps until the gate reaches a desired height (see figures 10-14).

The step of forming the source region comprises; forming an epitaxial layer onto an exposed horizontal surface of an uppermost epitaxial layer of the gate, while doping (in-situ doping) with a conductivity enhancing dopant (see column 13,lines 27-30).

The conductivity enhancing dopant is an n-type dopant selected from the group consisting of phosphorous or arsenic containing dopant.

Prior to the step of forming the elevated gate, a dielectric layer, i.e. an oxide layer, (24, 74) is removed from the substrate overlying the buried drain (see figures 2, 3, 16 and 17).

The step of forming the buried drain in the substrate comprises doping an area of the substrate with a conductivity enhancing dopant by ion implantation (see column 3, lines 48-52).

The conductivity enhancing dopant is an n-type dopant selected from the group consisting of phosphorous and arsenic dopant.

A plurality of elevated transistors are formed on the substrate so as to define an array of transistors (see column 8, lines 53-55-column 10, lines 28-31).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

14. Claims 1-8, 27-32, 35-37, 40-44, 46, 48-51, 54-63, 69-71 and 79-82 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. U.S. Patent 5,998,248.

Ma et al. discloses a method of forming a vertical structure (raised structure, source/drain, elevated structure or epitaxial structures) on a monocrystalline substrate 1, comprising the steps of; selectively growing a first epitaxial layer 7 of monocrystalline silicon on the substrate1; forming a layer 9 of an insulative material over the first epitaxial layer 7 (see figure 5); removing a portion of the insulative layer to expose only a top surface of the first epitaxial layer 7; and selectively growing a second epitaxial layer 11 of monocrystalline silicon on the exposed surface of the first epitaxial layer 7.

One or more epitaxial layers having thickness of about 70 to about 100 nm (see column 3, lines 57-61).

The vertical structure is a source or drain having a height of at least about 10 to about 30 nm.

Prior to the step of selectively growing the first epitaxial film, at least partially removing an oxide layer 5 from the substrate (see figures 2 and 3) by using an oxide dry etch (see column 2, lines 60-67).

The insulative layer comprises silicon oxide having a thickness of about 2 to about 5 nm (see column 3, lines 44-45).

The insulative layer is formed by annealing using rapid thermal oxidation (see column 3, lines 35-38).

The insulative layer is removed by reactive ion etching (see column 3,lines 55-56).

The vertical structure is formed adjacent to an existing gate 3 or word line on the substrate 1.

Ma et al. is applied as above but lacks anticipation on forming a layer of an insulative material over the second epitaxial layer; repeating the steps of removing a portion of the insulative layer, growing an epitaxial layer, and forming the insulative layer, until the vertical structure reaches a desired height, each of the epitaxial layers having insulated sidewalls, and an uppermost epitaxial layer of the vertical structure having insulated sidewalls and an insulated top surface; disclosing a crystalline plane orientation of the silicon substrate having a (100) plane orientation and a facet having a plane orientation of (100), (110), or (111); disclosing each epitaxial layer having a thickness of up to about 200 nm; removing the oxide layer by applying an oxide cleaning solution to the substrate; disclosing an oxide dry etch comprising exposing the substrate to an H2 gas at about 800°C. to about 850°C; using an oxide dry etch comprising exposing the substrate to a reactive plasma at about 100°C; exposing the epitaxial layer to a dry oxygen gas at a pressure of about 100 to about 200 Torr and temperature of about 800°C. to about 1200°C; and exposing the insulative layer to an etch gas in an ionized state, the etch gas comprising at least one fluorine-containing gas.

With respect to forming a layer of an insulative material over the second epitaxial layer, Ma et al. clearly suggest subjecting the device to conventional processing to provide a finished device (see column 4, lines 5-7), therefore it would have been obvious to a person having ordinary skills in the art at the time the invention was made to form a layer of an insulative material over the second epitaxial layer in the primary reference of Ma et al. since it would provide conventional device insulation.

Regarding repeating the steps of removing a portion of the insulative layer, growing an epitaxial layer, and forming the insulative layer, until the vertical structure reaches a desired height, each of the epitaxial layers having insulated sidewalls, and an uppermost epitaxial layer of the vertical structure having insulated sidewalls and an insulated top surface; it would have been obvious to a person having ordinary skills in the art at the time the invention was made to repeat these steps since it is conventionally performed in the art in order to obtain a device of a desire height.

With respect to disclosing a crystalline plane orientation of the silicon substrate having a (100) plane orientation and a facet having a plane orientation of (100), (110), or (111); it would have been obvious to one having ordinary skills in the art at the time the invention was made to disclose an orientation plane of 100 for the silicon substrate and an orientation plane of 100, 110 or 11 for the facets in the primary reference of Ma et al. since these are conventional and common plane orientation values of monocrystalline silicon substrates.

Regarding disclosing each epitaxial layer having a thickness of up to about 200 nm it is not patentable subject matter to discover the optimum thickness of a layer by optimizing using routine experimentation, therefore it would have been obvious to a person having ordinary skills in the art at the time the invention was made to form each epitaxial layer of up to about 200 nm in the primary reference of Ma et al..

With respect to removing the oxide layer by applying an oxide cleaning solution to the substrate, using an oxide cleaning solution to remove oxide layers is conventional in the art, therefore it would have been obvious to a person having ordinary skills in the

art at the time the invention was made to use an oxide cleaning solution to remove the oxide layer in the primary reference of Ma et al. since removing an oxide with an oxide cleaning solution is a conventional alternate method of removing an oxide in semiconductor manufacturing processes.

Regarding disclosing an oxide dry etch comprising exposing the substrate to an H2 gas at about 800°C. to about 850°C, performing oxide dry etching processes by exposing the substrate to an H2 gas at about 800°C. to about 850°C s a conventional alternate process for removing an oxide, therefore it would have been obvious to a person having ordinary skills in the art at the time the invention was made to use an oxide dry etch comprising exposing the substrate to an H2 gas at about 800°C. to about 850°C in the primary reference of Ma et al..

With respect to using an oxide dry etch comprising exposing the substrate to a reactive plasma at about 100°C, using reactive plasma at about 100°C to remove an oxide layer is an alternate process of removing oxides layers therefore it would have been obvious to a person having ordinary skills in the art at the time the invention was made to remove the oxide layer in the primary reference of Ma et al. by using reactive plasma at about 100°C.

With respect to forming the insulating layer by exposing the epitaxial layer to a dry oxygen gas at a pressure of about 100 to about 200 Torr and temperature of about 800°C. to about 1200°C; it is not patentable subject matter to discover the optimum process rages or parameters by using routine experimentation, therefore it would have been obvious to a person having ordinary skills in the art at the time the invention was

made to form the insulating layer in the primary reference of Ma et al. by exposing the epitaxial layer to a dry oxygen gas at a pressure of about 100 to about 200 Torr and temperature of about 800°C. to about 1200°C since these pressure and temperature parameters are conventional processing parameters of forming an insulating layer.

Regarding exposing the insulative layer to an etch gas in an ionized state, the etch gas comprising at least one fluorine-containing gas; etching an insulating layer using a fluorine containing gas is conventional in the art therefore it would have been obvious to a person having ordinary skills in the art at the time the invention was made to etch the insulating layer in the primary reference of Ma et al. using a fluorine containing gas.

15. Claims 9-23, 26, 61, 64-67 rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. U.S. Patent 5,998,248 in view of Nakabayashi U.S. Patent 6,319,782 B1.

Ma et al. is applied as above but lacks anticipation on disclosing a selectively growing the epitaxial process for growing the epitaxial layers comprising introducing a silicon-comprising gas over the substrate by heating the substrate to about 450°C to about 950°C, and flowing at least one silicon-comprising precursor gas over the substrate at a rate of about 10 to about 500 ccm, for about 15 to about 30 seconds; flowing a silicon-comprising gas over the substrate at a rate and pressure to provide a growth rate of the epitaxial layer at about 20 to about 40 nm/minute; disclosing a pressure of about 1 to about 20 Torr for the flowing process; flowing the silicon gas over

the substrate at a rate and pressure to provide a growth rate of the epitaxial layer at less than about 10 nm/minute; disclosing a flowing pressure is about 0.02 to less than about 1 Torr to provide a growth rate of the epitaxial layer at about 0.3 to less than about 10 nm/minute; disclosing a silicon-comprising gas is selected from the group consisting of silane combined with chlorine, disilane combined with chlorine, disilane combined with hydrochloric acid, dichlorosilane, silicon tetrachloride, and combinations thereof; introducing the silicon-comprising gas with a conductivity enhancing p-type dopant selected from the group consisting of diborane, boron trichloride, boron trifluoride, and combinations thereof; introducing the conductivity enhancing dopant at a variable rate to provide a concentration gradient of the dopant within the epitaxial layer; and introducing the gas at an increasing rate to provide a low to high concentration of the dopant within the epitaxial layer.

Nakabayashi discloses a method of forming monocrystalline silicon layers using the processing ranges, parameters, gases and dopants disclosed above; therefore it would have been obvious to a person having ordinary skills in the art at the time the invention was made to formed the monocrystalline silicon layers in the primary reference of Ma et al. by using the process disclosed by Nakabayashi because a layer of superior crystallinity can be formed (se Abstract).

16. Claims 2, 24, 25, 34, 38, 39, 50, 52, 53, 61, 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura U.S. Patent 6,391,692.

Nakamura et al. is applied as above but lacks anticipation on repeating the steps of removing a portion of the insulative layer, growing an epitaxial layer, and forming the insulative layer, until the vertical structure reaches a desired height, each of the epitaxial layers having insulated sidewalls, and an uppermost epitaxial layer of the vertical structure having insulated sidewalls and an insulated top surface; doping the uppermost epitaxial layer by ion implantation using a fluorine-comprising gas selected from the group consisting of PF_3, PF_5, AsF_5, and $B^{11}F_3$; disclosing an insulative layer having a thickness of about 5 to about 20 nm, annealing by rapid thermal nitridation to form a nitride insulative layer by exposing the epitaxial layer to ammonia or nitrogen gas at a pressure of about 100 to about 200 Torr and temperature of about 800°C. to about 1200°C,.

Regarding repeating the steps of removing a portion of the insulative layer, growing an epitaxial layer, and forming the insulative layer, until the vertical structure reaches a desired height, each of the epitaxial layers having insulated sidewalls, and an uppermost epitaxial layer of the vertical structure having insulated sidewalls and an insulated top surface; it would have been obvious to a person having ordinary skills in the art at the time the invention was made to repeat the steps of removing a portion of the insulative layer, growing an epitaxial layer, and forming the insulative layer, until the vertical structure reaches a desired height, each of the epitaxial layers having insulated sidewalls, and an uppermost epitaxial layer of the vertical structure having insulated sidewalls and an insulated top surface in the primary reference of Nakamura since a monocrystalline layer of a desire height may be obtained.

With respect to doping the uppermost epitaxial layer by ion implantation using a fluorine-comprising gas selected from the group consisting of PF_3, PF_5, AsF_5, and $B^{11}F_3$; it would have been obvious to a person having ordinary skills in the art at the time the invention was made to used a fluorine-comprising gas selected from the group consisting of PF_3, PF_5, AsF_5, and $B^{11}F_3$ to doped the uppermost layer of the primary reference of Nakamura since fluorine-comprising gases selected from the group consisting of PF_3, PF_5, AsF_5, and $B^{11}F_3$ are conventional used as alternate dopant gases of arsenic doped regions.

With respect to disclosing an insulative layer having a thickness of about 5 to about 20 nm, the specific thickness range claimed by applicant, i.e., 5 to about 20 nm, is only considered to be the "optimum" thickness disclosed by the Nakamura et al. that a person having ordinary skill in the art at the time the invention was made would have been able to determine using routine experimentation based, among other things, on the desired accuracy, manufacturing costs, etc. (see In re Boesch, 205 USPQ 215 (CCPA 1980)).

17. Claims 86, 87, 92, 94, 97, 98 and 100 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mazuré et al. U.S. Patent 5,308,782.

Mazuré et al. is applied as above but lacks anticipation on selecting the n-type dopant from the group consisting of phosphine, arsine, and combinations thereof; disclosing a doped area of the substrate of about 50 nm to about 100 nm wide; selecting the conductivity enhancing dopant from the group consisting of PF3, PF5,

AsF5, and combinations thereof; and forming shallow trench isolation regions in the substrate to isolate the transistor.

With respect to selecting the n-type dopant from the group consisting of phosphine, arsine, PF3, PF5, AsF5 and combinations thereof; Mazuré et al. discloses using phosphorous an arsenic containing dopants, therefore it would have been obvious to a person having ordinary skills in the art at the time the invention was made to disclosed using phosphine, arsine, PF3, PF5 or AsF5 as the dopant gases in the primary reference of Mazuré et al. since phosphine, arsine, PF3, PF5 and AsF5 are conventional phosphorous and arsenic containing doping gases.

Regarding disclosing a doped area of the substrate of about 50 nm to about 100 nm wide, Mazuré et al. discloses forming a trench of 0.5 micron or less (see column 3, lines 65-66); therefore it would have been obvious to a person having ordinary skills in the art at the tine the invention was made to disclosed a doped area of the substrate of about 50 nm to about 100 nm wide in the primary reference of Mazuré et al. since a range of 50 nm to about 100 nm can be obtained by routine optimization of the process disclosed by Mazuré et al..

With respect to forming shallow trench isolation regions in the substrate to isolate the transistor; it would have been obvious to a person having ordinary skills in the art at the time the invention was made to for isolation regions in the primary reference of Mazuré et al. since conventional desire isolation of the semiconductor device may be obtained.

Allowable Subject Matter

18. Claims 72-78 are allowed.

19. The following is an examiner's statement of reasons for allowance: The prior art either single or in combination failed to anticipate or render obvious the limitations of forming a DRAM cell on a silicon substrate by forming a gate structure as required by claim 72.

20. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Jastrzebski et al., Pfiester, Fitch et al., Rodder et al. and Hada disclose processes of fabricating semiconductor devices comprising vertically arranged monocrystalline silicon layers.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (703) 306-0207. The examiner can normally be reached on Monday-Friday 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

AR
June 17, 2002

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800